

Signal Rectification, using Switched Capacitor Modulators

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Associated Project: Yes

Associated Part Family: CY8C25xxx, CY8C26xxx

Summary

The unique configuration of the PSoC MCU switched capacitor blocks allows construction of analog modulators. A detailed explanation of their function is provided showing how to rectify analog signals. Expanding these ideas allows designers to combine an analog modulation with a Low Pass Filter (LPF2) to build an amplitude demodulator.

Introduction

Many applications require rectifying analog signals. Normally this is done with diodes. PSoC microcontrollers do not have signal diodes available for analog functions. Instead of diodes, it has modulators; a much better solution! This Application Note provides:

- A brief explanation of analog modulation with the switched capacitor blocks.
- An example of an analog rectifier.
- An example of an amplitude demodulator built with an LPF2 Low Pass Filter User Module.

For background on switched-capacitor design, please review Application Note [AN2041](#) "Understanding Switched Capacitor Blocks."

Analog Modulation

Equation (1) shows that analog modulation requires multiplying an input signal by some function:

$$m(v_{in}(t)) = v_{in}(t) * f(t) \quad (1)$$

Multipliers are not cheap, but if $f(t)$ is limited to a function containing only values 1 and -1, the modulation Equation (1) reduces to the more manageable Equation (2) :

$$m(v_{in}(t)) = \begin{cases} v_{in} & ; f(t) = 1 \\ -v_{in} & ; f(t) = -1 \end{cases} \quad (2)$$

The multiplier reduces to an amplifier with selectable gain polarity.

Switch Cap Blocks as Modulators

Figure 1 shows a switched capacitor block configured as an amplifier.

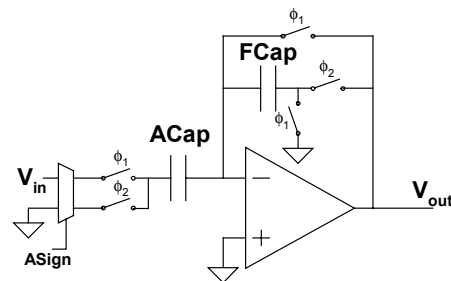


Figure 1: Selectable Gain Polarity Amplifier

The gain polarity is determined by whether V_{in} is sampled during the acquisition phase (ϕ_1) or the charge-transfer phase (ϕ_2). **ASign** controls timing of these switches. Equation (3) shows the gain as a function of **ASign**:

$$\frac{V_{out}}{V_{in}} = \begin{cases} \frac{ACap}{FCap} & ; ASign = 0 \\ -\frac{ACap}{FCap} & ; ASign = 1 \end{cases} \quad (3)$$

[Appendix A](#) shows that **ASign** is bit 5 of Control Register 0 for a given SCBlock.

It is possible to modulate a signal using software to repetitively toggle the **ASign** bit. Such a solution requires high software overhead and would be limited to only the slowest modulation rates. Most modulation requires hardware.

- Input signals less than AGND to set the comparator and global output low causing the gain to remain negative. A negative input signal results in a positive output signal.
- Inputs equal to AGND leave the comparator and global output either high or low. For either case, the input is zero causing the output to also be zero. Whether it is plus or minus zero is an exercise left to the user.

A copy of the project associated with this Application Note can be found on our web site. [Appendix C](#) shows the User Module placement for this application.

A 2Vpp input around AGND at 1 kHz is input to this circuit. Figure 5 shows input on the upper waveform and the output on the lower waveform.

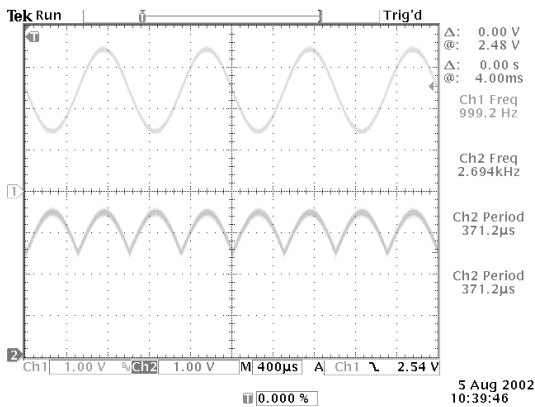


Figure 5: Rectifier Waveforms

It is apparent the output is the rectified input.

Theme and Variation

Reconfiguring SCBuffer to have a positive gain results in the waveforms shown in Figure 6.

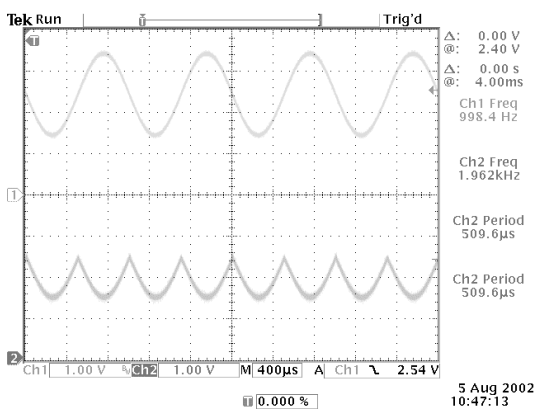


Figure 6: Negative Rectifier Waveforms

The output is now the negative rectification of the input.

But Wait, There's More!

Figure 7 shows a variation where the BCap is also connected to the input.

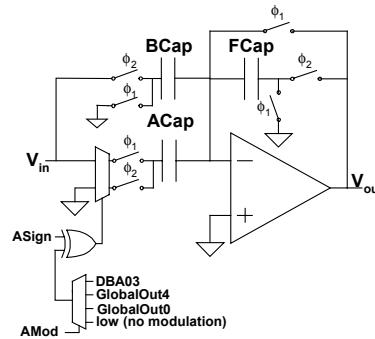


Figure 7: SCBlock Modulator with Extra Input

Equation (4) shows the relationship of V_{out} to V_{in} when...

- the ACap is connected to the input with a gain of $-1/2$,
- the BCap is connected to the input with a gain of $-1/2$,
- and the Modulator is enabled.

$$v_{out} = \frac{abs(v_{in})}{2} - \frac{v_{in}}{2} = \begin{matrix} 0 & ; v_{in} \geq 1 \\ -v_{in} & ; v_{in} < -1 \end{matrix} \quad (4)$$

Figure 8 shows the parameter selection to implement the SCBlock shown in Figure 7.

User Module Parameters	
FCap	32
ClockPhase	Norm
ASign	Neg
ACap	16
ACMux	ACA00
BCap	16
AnalogBus	AnalogOutBus_0
CompBus	Disable
AutoZero	On
CCap	0
ARefMux	AGND
FSW1	On
FSW0	On
BMux	ACA00
Power	High

Figure 8: Parameter Selection for 2 Input SCBuffer

Figure 9 shows the output to be a half-cycle rectification of the input.

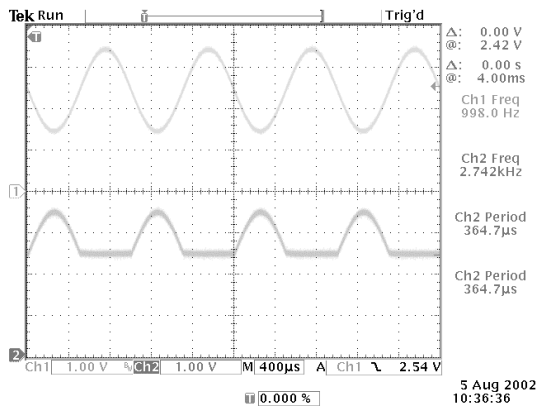


Figure 9: Positive Half-Cycle Rectifier Waveforms

Similarly, Figure 10 shows a half-cycle rectifier in the opposite direction when the SCBlock gain is set to $+\frac{1}{2}$.

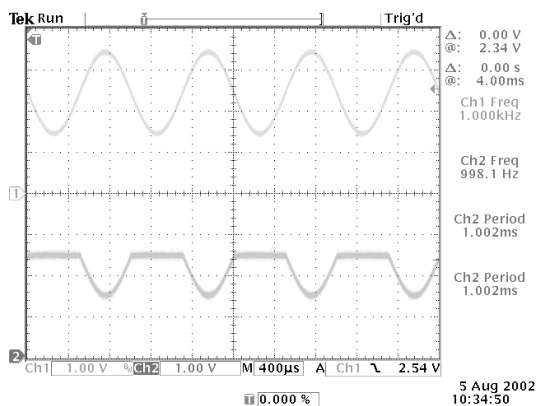


Figure 10: Negative Half-Cycle Rectifier Waveforms

Amplitude Demodulation

Figure 11 shows a high level diagram of a traditional amplitude demodulator. An input signal is rectified and passed to a Low Pass Filter.

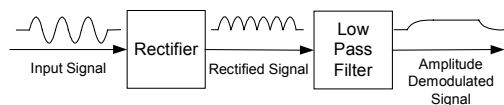


Figure 11: Conventional Amplitude Demodulator

You can build it this way if you wish. You'll be forced to if you use conventional circuitry, but you aren't using conventional circuitry.

Creating an amplitude demodulator requires a low pass filter. PSoC Low Pass Filters are made of two SCBlocks. A Type A SCBlock connects the input signal while a Type B SCBlock supplies the output. The **ASign** bit of the Type A SCBlock controls the polarity of the filter's gain.

If the filter is placed so that the input block is either **ASA10** or **ASA12**, then the modulator can be built right into the Low Pass Filter. Figure 12 shows the simplified block diagram.

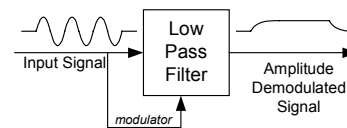


Figure 12: PSoC Amplitude Demodulator

Build an Amplitude Demodulator

For this example the amplitude modulated signal has a carrier frequency of 52 kHz. Its amplitude is modulated with a signal having a bandwidth no larger than 3 kHz.

Figure 13 shows a block diagram for an amplitude demodulator.

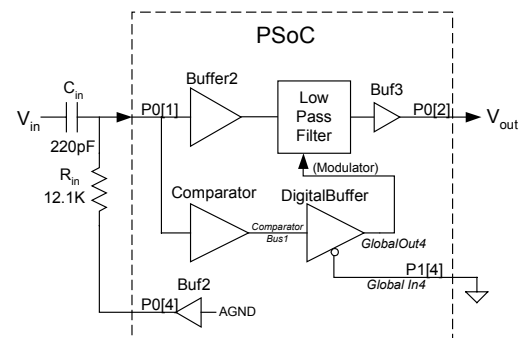


Figure 13: Amplitude Demodulator Block Diagram

The input passes through an external 25 kHz Single Pole High Pass Filter. The signal comes in on Port 0[1] to a buffer and a comparator. Buffer2 is a Programmable Gain Amplifier (**PGA_A**) User Module configured to have a gain of one. The comparator is a Programmable Threshold Comparator (**CMPPRG**) User Module with its threshold set to $V_{cc}/2$ (AGND). Its output is connected to the column comparator bus 1. The digital buffer is a SPI Slave (**SPIS**) User Module configured to connect the column comparator 1 to Global Output 4. Pulling Port 1[4] to ground enables its output.

The parameters for the Low Pass Filter are shown in Figure 14:

User Module Parameters	
AnalogBus	AnalogOutBus_3
C1	1
C2	1
C3	2
C4	31
CA	32
CB	32
Input	ACA02

Figure 14: Parameters for a Butterworth Low Pass Filter

These parameters configure this filter to be a Two-Pole Butterworth Low Pass Filter having a corner frequency of the column clock divided by 558. For this application, the column clock is 2 MHz making the corner frequency 3.6 kHz. (Note: These parameter settings make a good general-purpose Low Pass Filter. Copy this page and pin it on the wall. A 1 kHz filter requires a column clock of 558 kHz. That's 24MHz/43. Now add to your resume that you have proficiency in filter design.) The gain is determined by C_1/C_2 and set to one. C_1 's contribution is only to set gain and not affect the corner frequency or damping ratio. The user may select any gain value from 0 to 31 in incremental steps of 1. The filter's output connects to the analog output buffer on Port 0[2].

It is necessary to enable the modulator for SCBlock ASA12 in the low pass filter. The code segment below shows how:

```
/Enable modulator for ASA02
M8C_SetBank1
or reg[AMD_CR],08h ;GlobalOutput[4]
M8C_SetBank0
```

The Analog Modulator Control Register (AMD_CR) is in register Bank 1. When AMD_CR is set to xxx10xxb, Global Output 4 controls the modulator for ASA12.

Analog ground reference can be generated using the RefMux User Module and the analog column buffer or by setting the TestMux bits in Buffer 2 (ACA02) using the following code segment:

```
//Connect AGND to AnalogBus
// to AGND
or reg[Buffer2_GAIN_CR2],14h
```

Except for starting the User Modules, no other software control is needed.

Amplitude Demodulator Gain

Figure 11 showed an amplitude demodulator to be a rectifier followed by a Low Pass Filter. Figure 15 shows a rectified sinusoid:

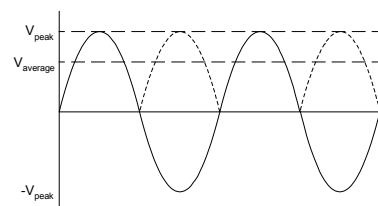


Figure 15: A Rectified Sinusoid and its Average

The Low Pass Filter will filter this rectified signal to produce an average signal. Equation (5) shows the average of a rectified sinusoid to be about 64% of its peak value:

$$v_{average} = \frac{1}{\pi} \int_0^{\pi} v_{peak} \sin(t) \delta t = \frac{2}{\pi} v_{peak} \quad (5)$$

This gain factor must be taken into account when determining the total gain of the entire signal path.

A carrier signal of 52 kHz is modulated with a 3 kHz signal to produce a 2 Vpp 80% modulated signal. Figure 16 shows this input on the upper waveform and the demodulated output on the lower waveform:

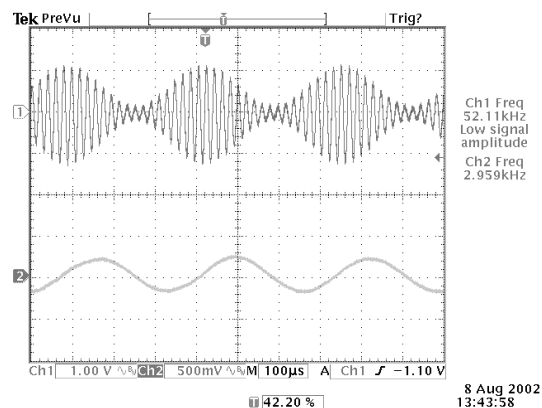


Figure 16: Waveforms for an 80% Modulated Carrier

The phase delay between the output and the input envelopment results from the 3.6 kHz Low Pass Filter.

Figure 17 shows an input waveform of a 10-cycle burst of 52 kHz and its demodulated output.

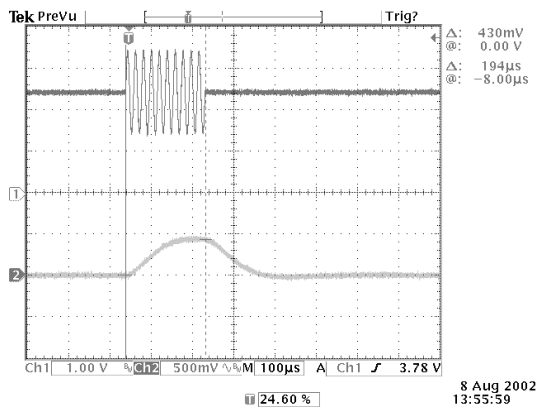


Figure 17: Waveforms for 10-Cycle Burst of Carrier

Again, the delay in the demodulated output is the result of the low pass filter.

Conclusion

The PSoC switched capacitor architecture is greatly enhanced with the addition of built in modulators. These modulators allow seamless construction of analog rectifiers and amplitude demodulators. Always options, never grief.

[Appendix A](#)

Control Registers for a Type A Switched Capacitor Block

[Appendix B](#)

Analog Modulator Control Register

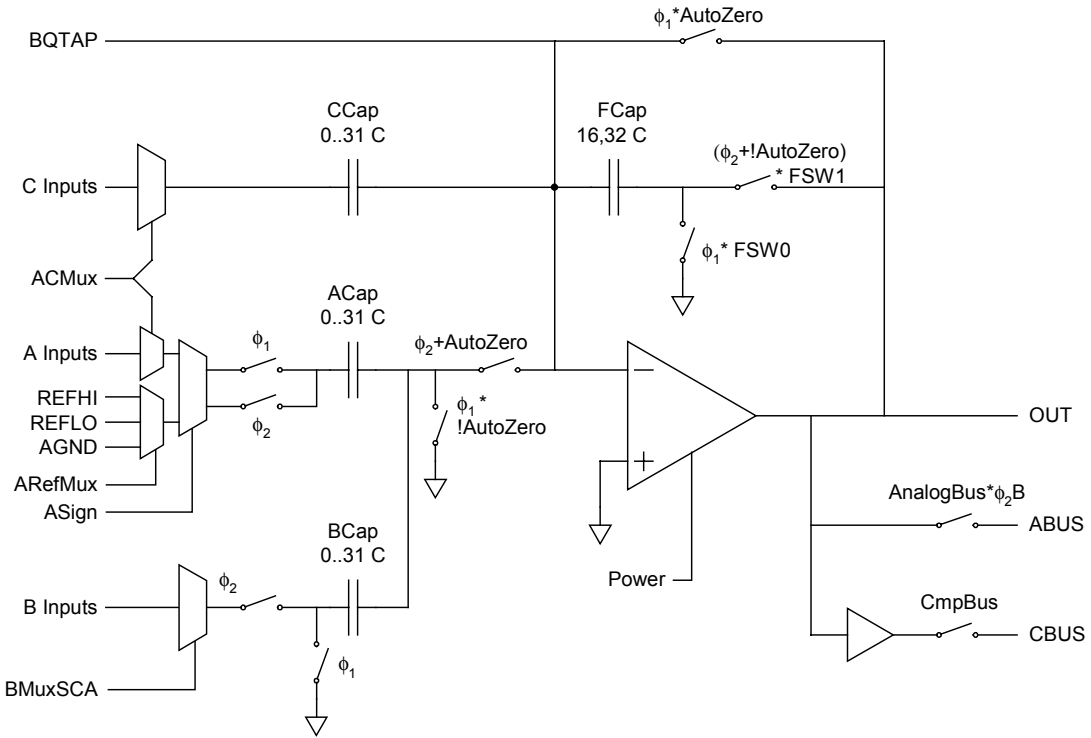
[Appendix C](#)

User Module Placement View for Attached Project

Appendix A

Control Registers for a Type A Switched Capacitor Block

	7	6	5	4	3	2	1	0
CR0	FCap 16, 32		ClockPhase Norm, Swap	ASign Pos, Neg	ACap [0..31]			
CR1	ACMux C: North => A: North, E1W2, REFHI, South; C: Diag => A: Diag, Diag, Diag, Diag				BCap [0..31]			
CR2	AnalogBus Disable, Enable	CompBus Disable, Enable	AutoZero Off, On	CCap [0..31]				
CR3	ARefMux AGND, REFHI, REFLO, CMP		FSW1 Off, On	FSW0 Off, On	BMuxSCA North, E1W2, E2W1, South		Power Off, Low, Med, High	



Appendix B

Analog Modulator Control Register

Bit #	7	6	5	4	3	2	1	0
POR	0	0	0	0	0	0	0	0
Read/ Write	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	Reserved	Reserved	Reserved	Reserved	AMOD2[1]	AMOD2[0]	AMOD0[1]	AMOD0[0]

Bit 7: Reserved
Bit 6: Reserved
Bit 5: Reserved
Bit 4: Reserved

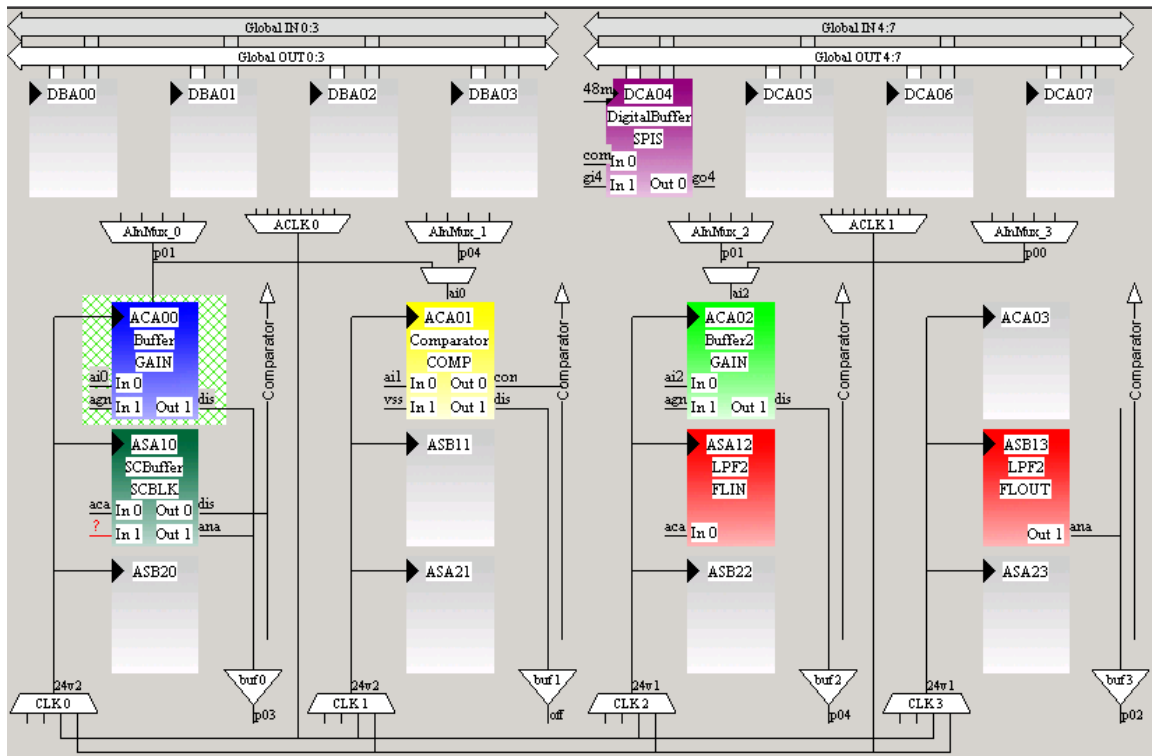
Bit [3:2]: AMOD2[1], AMOD2[0] Selects the modulation signal for Analog Column 2
 0 0 = No Modulation
 0 1 = Global Output [0]
 1 0 = Global Output [4]
 1 1 = Digital Basic Type A Block 03

Bit [1:0]: AMOD0[1], AMOD0[0] Selects the modulation signal for Analog Column 0
 0 0 = No Modulation
 0 1 = Global Output [0]
 1 0 = Global Output [4]
 1 1 = Digital Basic Type A Block 03

Analog Modulator Control Register (AMD_CR, Address = Bank 1, 63h)

Appendix C

User Module Placement View for Attached Project



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