Application Note AN2300

Non-Volatile Memory Controller with Realtime Clock

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PSoC Designer Version: 4.2

Abstract
This Application Note describes a PSoC™ non-volatile memory controller. It is used to retain the values in the CMOS SRAM for long periods of time when the primary power supply is disconnected or falls below the minimum specified voltage. This design uses a battery as the secondary power supply. Also, a realtime clock is included for a very robust solution.

Introduction
The non-volatile memory controller (NVMC and realtime clock (RTC) have one common feature. Both require alternative power to operate when the main power is turned off. Therefore, combining a NVMC with an RTC in one device is a logical solution.

Non-Volatile Memory Controller
The main goal of a non-volatile memory controller is to switch the CMOS SRAM power to a battery and disable the memory writes by blocking the memory chip-enabled (CE) signal.

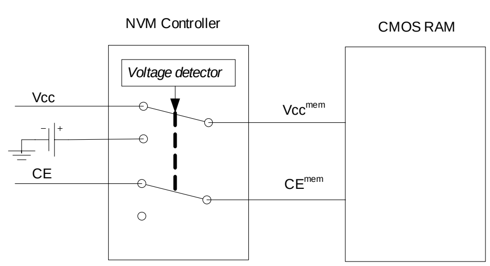

Figure 1. NVMC Logical Structure

The main task of the NVMC is to detect power failures and power restorations using minimal current consumption. This preserves battery life.

The typical way to detect power failures and power restorations is to use a comparator. But in this case we don't want the battery to provide the power consumed by the reference and analog buffer. Therefore, in this design we use low voltage detection (LVD) and the switch mode pump (SMP). The LVD's threshold and the SMP's start values are set in the same register. The SMP start value is always greater than the LVD threshold value. The LVD interrupt is used to detect power failures when the power falls below the pre-defined threshold. The SMP pin is set as open drain low that starts as a short to ground (high frequency short) when the power falls below the pre-defined level. The SMP stops oscillating to ground when the voltage returns to above the pre-defined level (power back to normal). Using this pin with one capacitor and one resistor we can get a logical 0 when power is below the SMP start voltage and a logical 1 when the supply voltage is greater than SMP start voltage (see Figure 2).

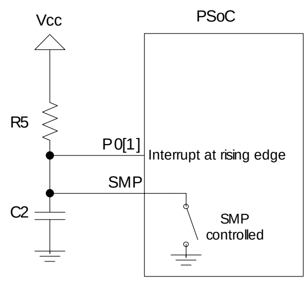

Figure 2. Using the SMP to Detect Power

Capacitor C2 is charged slowly by the small current through R5 and is almost instantly discharged by the SMP-controlled switch. Therefore, when the SMP is working, P0[1] holds a logical low level. After the SMP stops working, C2 charges to logical high level and P0[1] generates a rising edge interrupt. In this way, the power restoration is detected.

When the interrupt from the LVD occurs, the PSoC switches itself and the CMOS SRAM to battery power, blocks the CE signal, and goes into sleep mode. P0[1] interrupt wakes up the processor, unlocks the CE signal, and switches back to normal power. The difference between the LVD threshold value and the SMP start value adds some hysteresis that increases system stability. Figure 3 shows the operational waveform when power failure occurs. The abbreviations are as follows:

- Vcc – main supply
- SMP – value on the PSoC SMP pin
- CE_{OUT} – output signal
- V_{SMP} – power supply voltage value caused by the start of the SMP
- V_{LVD} – power supply voltage value that triggers the LVD interrupt
- $V_{"1"}$ – value that identifies a logical high
- V_{Q1drop} – voltage drop on Q1's built-in body diode when Q1 is turned off

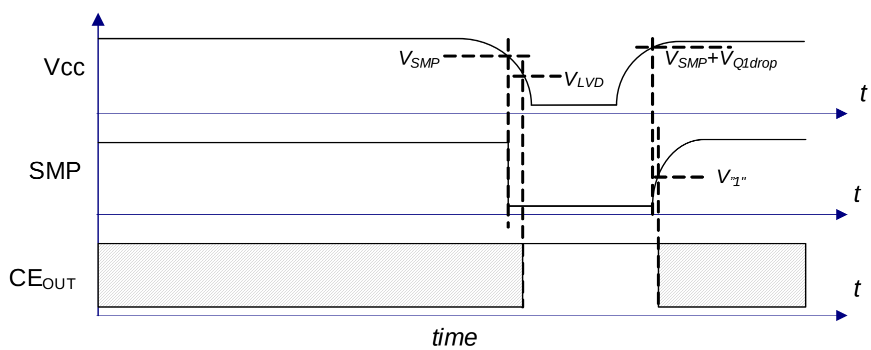

Figure 3. Power Failure Waveform

Realtime Clock

As mentioned above, the RTC is combined with the NVMC in the same device. Because the internal oscillator's (ILO) precision is not enough to build the RTC, an external 32.768 kHz crystal is used. The sleep timer generates a 1 Hz interrupt that is used to clock the timer.

The RTC software is very simple. The date/time data is stored in an array. Each byte of the array represents seconds, minutes, hours, days, months and years, respectively. The year represents the year count since 2000. Therefore, 2005 is stored as 05. The 1s interrupt handler increases the second's value. If the second's value is equal to a whole minute (60s), then the second's value is cleared and the minute's value is increased. If the minute's value is equal to a whole hour, the hour is increased and the minutes are set to zero.

This process is the same with days, months, and years. There is only one issue with increasing the month; months do not have equal days. This is why the day count array and the simple leap-year-detection algorithm are used. If the year divides by four (two least significant bits are zero) and the year value is not equal to 100 and 200, then the year is a leap year and the February day count is increased by one.

The RTC uses the I2C interface. It is realized as an I^2C slave device with an address of 40 (addresses can be freely modified in the I2C User Module parameters). The packets for reading and writing are very simple (see Figure 4).

sec	min	hour	day	mon	year

Figure 4. I2C Packet for Time/Date Data Exchange

The I2C master device can read and/or write a partial or whole packet. The master device obtains time data by reading the first three bytes. Similarly, it can write the time and not change the date by writing to the first three bytes.

Device Schematic

The device schematic is shown in Figure 5.

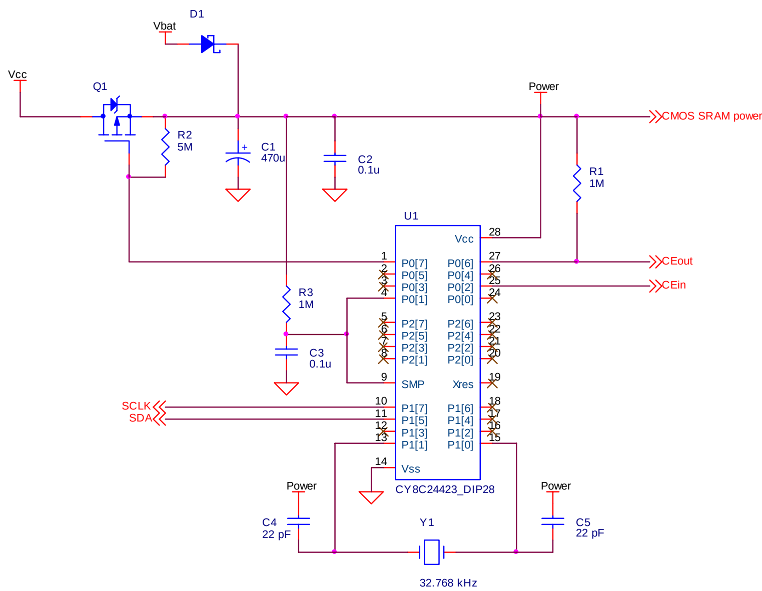

Figure 5. NVMC+RTC Schematic

Vcc is a standalone power source. *Power* is the derived power source for the PSoC and CMOS RAM. *CEout* is the external pull-up pin used to connect the RAM chip. *CEin* is the input pin for the memory CE signal. The Shottky diode D1 is used to prevent battery charging. The forward drop on D1 is low due to the RAM current consumption when inactive and the low PSoC current consumption when in sleep mode. Q1's internal diode detects the presence of standalone power when Q1 is turned off. The voltage drop when the Q1 internal diode is turned off increases the threshold between "good" and "bad" voltage values. For normal operation of PSoC and CMOS RAM in active mode, the MOSFET Q1 must be turned on in order to decrease the voltage drop on the internal diode. When Vcc is present and Q1 turned on, D1 is reverse biased and no current is pulled from the battery.

Using the CY8C21xxx PSoC Series

All the design functionality can be implemented on a CY8C21xxx PSoC device except this device has no dedicated pin to use the external crystal oscillator. A possible solution is to build a low-power external oscillator using an external transistor. The external oscillator generates a 32.768 kHz clock signal. The internal PSoC 16-bit counter is then used to divide the frequency and provide 1s intervals in place of the sleep timer used in the CY8C24xxxA-based design. The schematic for the CY8C21xxx-based design is shown in Figure 6.

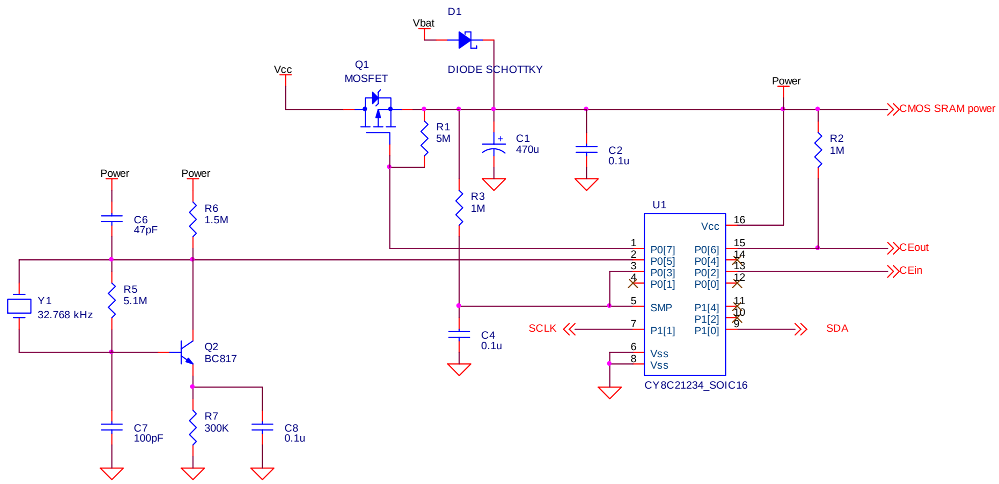

Figure 6. CY8C21xxx-Based NVMC+RTC Design Schematic

Test Results

The main goal of testing is to measure power consumption of the device in active and sleep modes. The results of the measurements are shown in Table 1.

Table 1.

Part	Active Mode	Standby
CY8C24423A	2.3 mA	10 uA
CY8C21234	6.1 mA	4 uA

About the Author

Name: Svyatoslav Paliy

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Background: Svyatoslav earned his Masters of Science diploma in 2000 from National University “Lviv Polytechnic“ (Ukraine). His interests include programming for various embedded, Windows and Linux systems.

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