Application Note AN2302

6-Channel DMX Dimmer

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Associated Part Family: CY8C27443
PSoC Designer Version: 4.2
Associated Application Notes: None

Abstract

Basic principles of 6-Channel DMX Dimmer operation are described in this Application Note. A DMX dimmer can be used to control the brightness of remote lighting in theaters, discos, and concert halls. The device is controlled via a DMX interface. The structure, device function algorithm, interconnection circuits, DMX Protocol, and fundamental design aspects based on the PSoC™ device are considered.

Introduction

Nowadays computer-controlled equipment techniques, consoles, and control panels are used to control effects and stage lighting in theatres, discos, concert halls, etc. The DMX Dimmer is used to convert the device input signal into an analog representation of lamp brightness (power).

The DMX Dimmer has the following characteristics (see Table 1).

Table 1. 6-Channel DMX Dimmer Characteristics

Number of Channels	6
Lamp Power	Depending on TRIAC Used
Power Supply	DC 5V, 100 mA
AC Synchronization	AC 110-220V, 47-63 Hz, Automatic Turning
Address Range	From 1 to 512
Service Features	DMX Bus Sleep-Mode Support

DMX Protocol

DMX protocol was established by the United States Institute for Theatre Technology (USITT) in 1986. This protocol represents standard interface for data communication between devices that are used for lighting. In 1990, revisions were made and now the protocol is known as USITT DMX512.

The DMX protocol uses the RS485 standard, which defines electrical interface, voltage, and current.

This standard supports receiver and transmitter "ground" connection to the cable core screen in order to lower the influence of external noise and improve electrical safety.

But the values of transmitter and receiver “ground” line voltage can be different, which causes current to pass through the cable screen. If the value of this current is too great, the DMX cable and the circuit can be destroyed.

In order to correctly work devices that use DMX, to control the interface, and also improve usage safety, it is necessary to implement galvanic isolation on the DMX receiver devices.

The DMX data stream is passed in the form of a burst that is repeated continually. This data burst consists of the synchro preamble that informs the receiver when it starts.

This stream contains the values of each channel from 1 to 512, or less (see Figure 1, Table 2). The bit rate in the DMX protocol is 250 kB. So, the duration of every bit is 4 µs. The number of channels passed is not fixed, but is limited by the standard, which is from 24 to 512.

If the information is given over all 512 channels, then the maximum frequency that the information is updated is at 44,115 Hz. The maximum frequency that the information is transmitted can be 836 Hz, which corresponds to 24 channels. Upon a long signal delay (more than 1s), the device can enter DMX sleep mode.

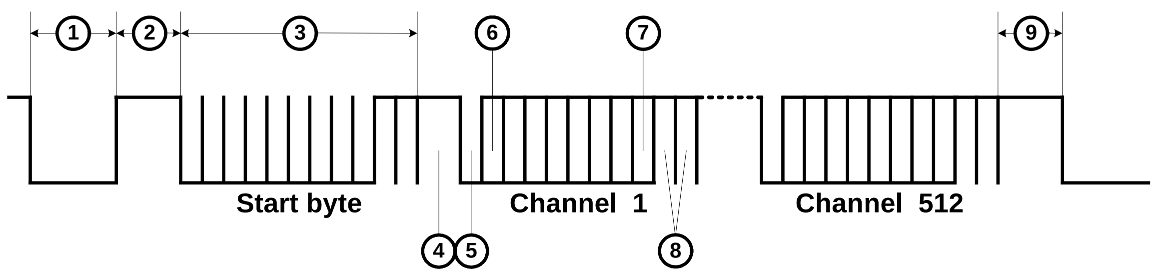


Figure 1. Structure of a DMX512 Signal

Table 2. Data Stream Description and Duration

Item	Description	Duration
1	Space for Break (Reset)	Min. 88 µs
2	Mark After Break (MAB)	8 µs – 1s
3	Slot Time	44 µs
4	Mark Time Between Slots	0 µs – 1s
5	Start Bit	4 µs
6	Least Significant Data Bit	4 µs
7	Most Significant Data Bit	4 µs
8	Stop Bit	4 µs
9	Mark Before Break (MBB)	0 µs – 1s

Lamp Power Phase Control

The TRIAC and lamp interconnection circuit example is shown in Figure 2. This setup allows the control of lamp brightness by varying the delay between AC line zero-crossing and TRIAC ON events (Figure 3). When control impulses are sent to the TRIAC, it switches to ON state. The TRIAC OFF state is automatically triggered when the voltage falls to zero at the next zero-crossing event.

Note that the dimmer can be used with varying AC frequencies; therefore, the AC line frequency needs to be measured in order to provide correct dimmer operation regardless of the actual power supply parameters.

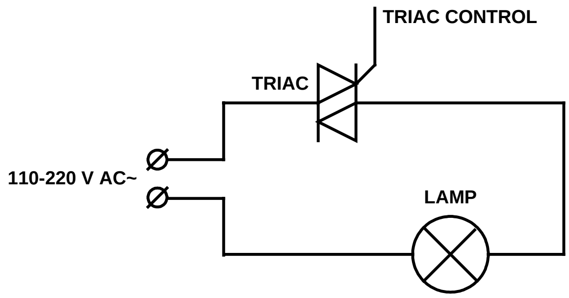


Figure 2. TRIAC and Lamp Interconnection Circuit Example

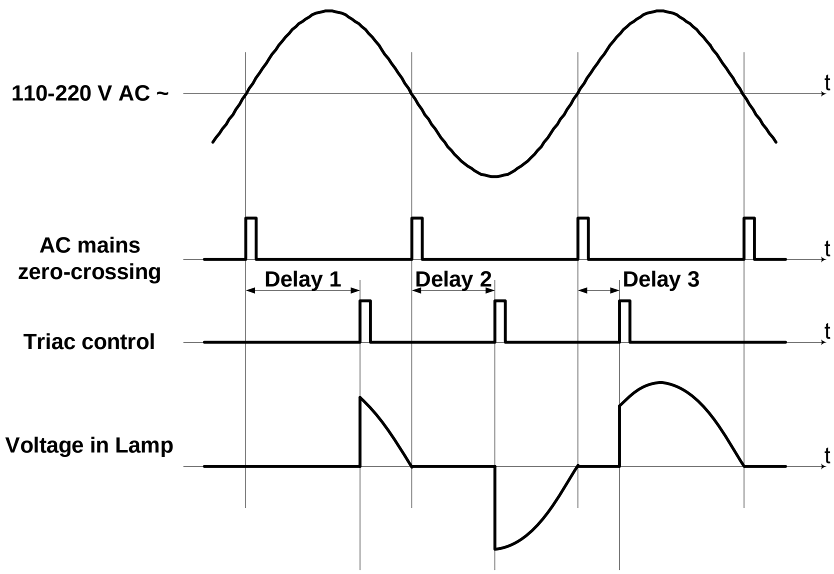


Figure 3. Timetable of Lamp Power Phase Control

DMX Dimmer

The DMX Dimmer block diagram is shown in Figure 4. The *DMX Receiver* receives data in accordance to the preset address range and translates them in the *TRIAC Control Unit.* When the value of the voltage is zero, the AC *Synchronizer* (zero-crossing detector) generates the lockout pulses that are used to delay initialization of the counters.

The *TRIAC Control Unit* has 6 independent counters. When the lockout pulse enters from the AC *Synchronizer*, the counters start their operation. If the counter reaches the preset brightness compare value, the control impulse for the TRIAC ON event is generated to turn the TRIAC on.

Note that the power supply of the AC *Synchronizer* and lamp must be the same.

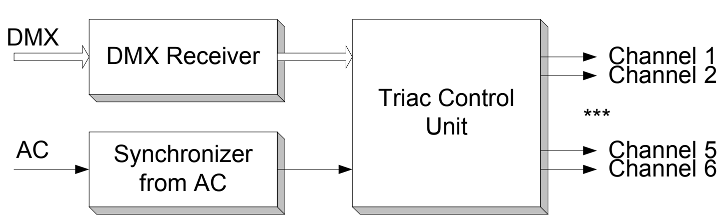


Figure 4. DMX Dimmer Block Diagram

DMX Dimmer Operation

Figure 5 illustrates the DMX Dimmer circuit.

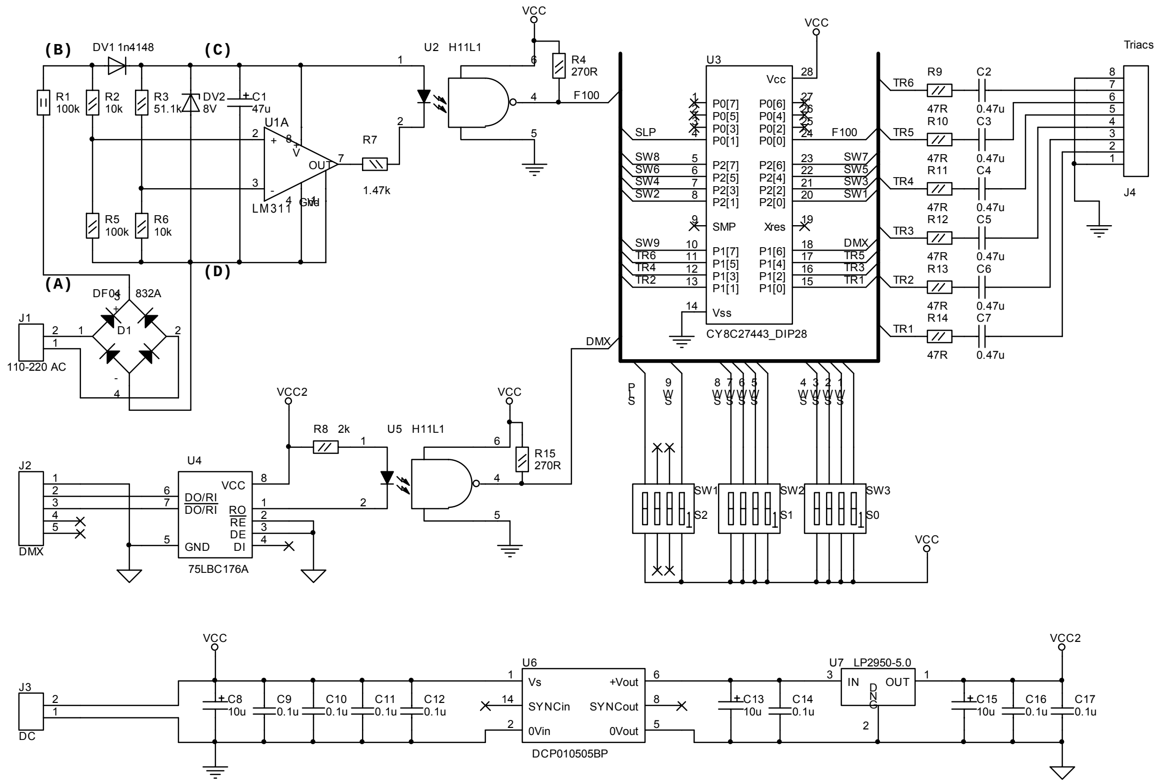


Figure 5. DMX Dimmer Circuit

In order to isolate the high voltage section from other parts of the circuit, it is necessary to do galvanic isolation using the optoisolator, U_2 H11L1.

Zero-crossing detection is implemented using U_1, a low-cost LM311 comparator. At Point "A" (after the diode bridge), the voltage is in the form of a fully-rectified sinusoid (Figure 6).

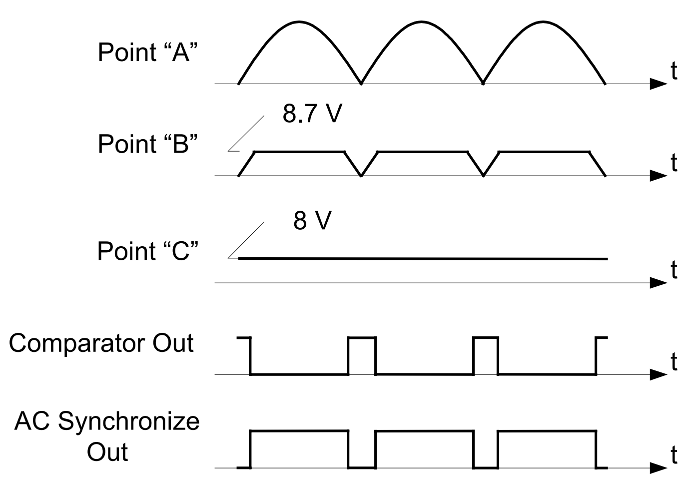


Figure 6. Clocking Unit Voltages of Points A, B, C Relative to Point D

The zener diode DV_2 and capacitor C_1 forms the 8V DC level relative to point «D». Voltage is scaled down to 1.3V by the voltage divider formed from R_3 and R_6. The 1.3V is used as a reference for negative comparator input. In point «B», voltage is in the form of a fully-rectified sinusoid. Voltage is supplied on positive input of the comparator by the voltage divider across R_2 and R_5. The comparator detects zero-crossing events and transmits them via the optocoupler, U_2.

The complexity of zero-crossing detection is compensated for by stable and reliable operation, noise-immunity, and testing in many industrial applications, including automated welding machines.

The DMX receiver operates from PSoC's RX8 receiver and Counter8 (Figure 7). The signal is supplied for the RX8 receiver and Counter8 through the RS485 differential receiver, U_4 75LBC176A, and the optocoupler, U_5. In order to provide galvanic isolated power supply for the U_4 receiver, the U_6 DCP010505BP DC/DC converter and U_7 low-drop LP2950-5.0 DC regulator are used.

The TRIAC control unit is built using PWM generators and the output signal is differentiated using a first order RC high pass filter.

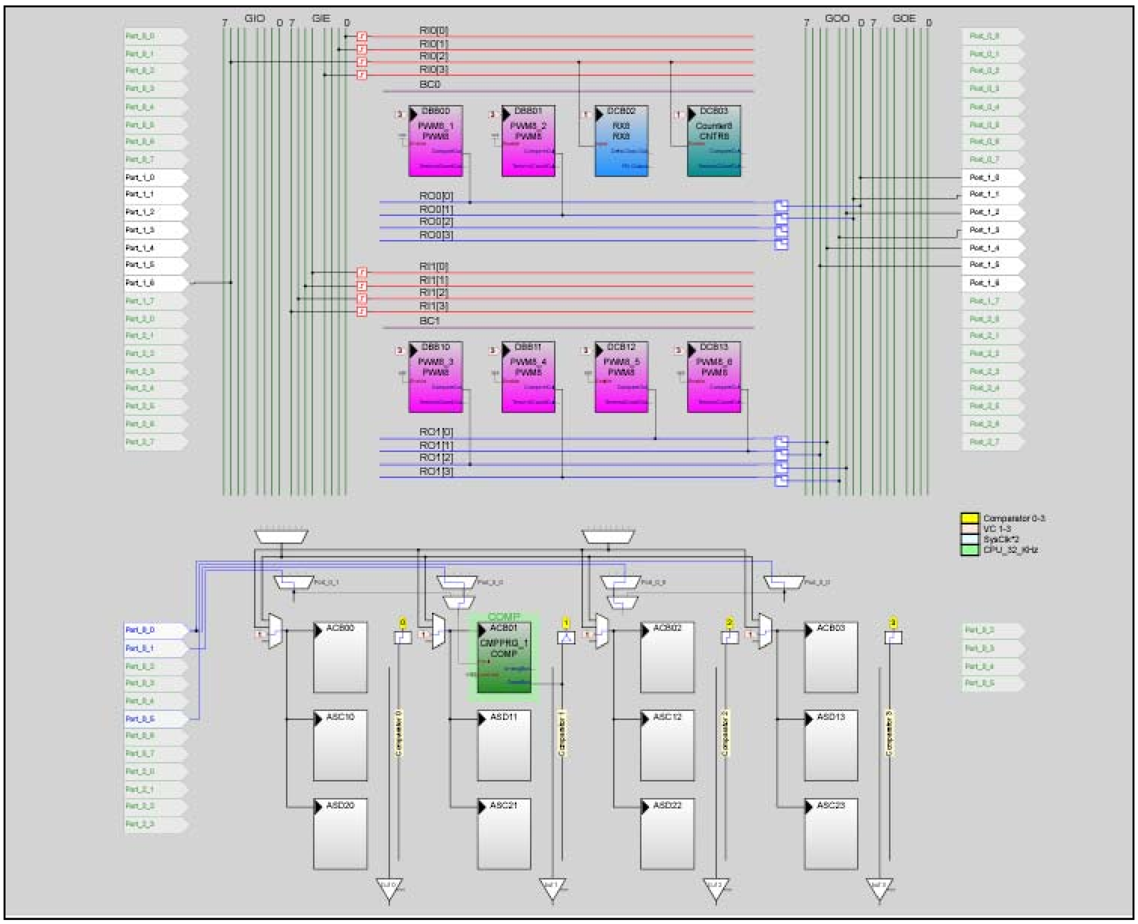
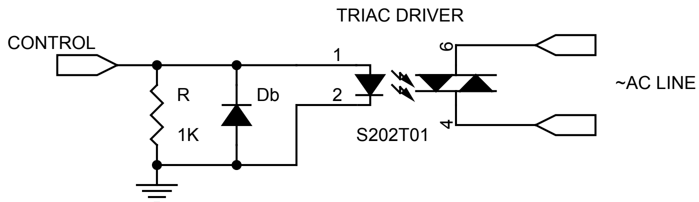


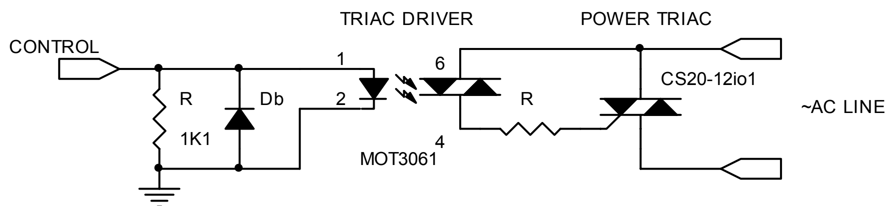
Figure 7. PSoC Internal User Module Configuration

It is important to provide good heat sink for the TRIACS, which are used to control the power lamp. This is why they are placed outside the PCB.

Figure 8 shows two different TRIAC circuits (depending on lamp power, low or high). The TRIAC, with a built-in optocoupler, is used for the galvanic isolation control circuit. This isolates the circuit from the power circuits. Diode D_b provides differential network capacitor discharge.



(a)



(b)

Figure 8. TRIAC Interconnection Circuit
(a) Low Lamp Power, (b) High Lamp Power

SW_1, SW_2, and SW_3 are used to set the address of the device and enable DMX bus sleep mode. The maximum number of channels specified by the DMX512 Protocol is 512. The starting channel address is set by 3 DIP switches, described as follows:

SW1/1 – is the address MSB, bit 8,
SW2/4 – 7,
SW2/3 – 6,
SW2/2 – 5,
SW2/1 – 4,
SW3/4 – 3,
SW3/3 – 2,
SW3/2 – 1,
SW3/1 – is the address LSB, bit 0.

SW1/2 and SW1/3 – are reserved.

SW1/4 is used to set DMX bus sleep mode. If there is no signal on the DMX line for more than 1s, (see the DMX Protocol), sleep mode activates and all lamps are switched off. If sleep mode is not enabled, the device continues to power itself at the lamp's last values of brightness (power).

The DMX receiver receives the signal on the RX8. The Counter8 is used to detect the break signal, the duration of which is at minimum 88 µs. The DMX line is sent on the RX8 receiver and Counter8 simultaneously (see Figure 7). The break signal is detected by triggering a counter interrupt. The GPIO interrupt is used to reset Counter8. The GPIO interrupt is activated from the same DMX line. RX8 chooses the data bytes from the DMX bus, and increments the software channel counter.

CMP comparator is used to generate zero-crossing interrupts, because the GPIO interrupt resource is already taken and PSoC has no dedicated flag registers to determine which GPIO pin triggered the interrupt.

Program Operation

The data are received in real-time from the DMX line and TRIAC control unit. That is why it is very important to separate these functions. If one of these functions misses its specified deadline, faulty operation can occur.

Using the software PWM to control the TRIACS is not an optimal solution. Program operation is based on processing short interrupts. When there is no active interrupt handling, the device is waiting but inactive. The duration of the data burst, which is received by the RX8, is only 44 μs.

With the PSoC system clock (IMO) of 24 MHz, the data burst takes 1056 cycles. The sum of the interrupt handler execution times must be less than this time. Five sources of interrupts are used (see Table 3). To minimize their duration they are written in assembly.

Table 3. Interrupt Sources

#	Source	Type	IMO Cycles (Maximum)
1	Counter8	Terminal Count	35
2	RX8	Receiver Full	284
3	GPIO	Rising Edge	23
4	Analog Column1	Rising Edge	193
5	Sleep Timer	Terminal Count	78

The PSoC initialization flowchart is shown in Figure 9. Initialization consists of two functions. First, AC line frequency calibration occurs and second, initialization of variables and modules occurs. These variables are necessary for device operation.

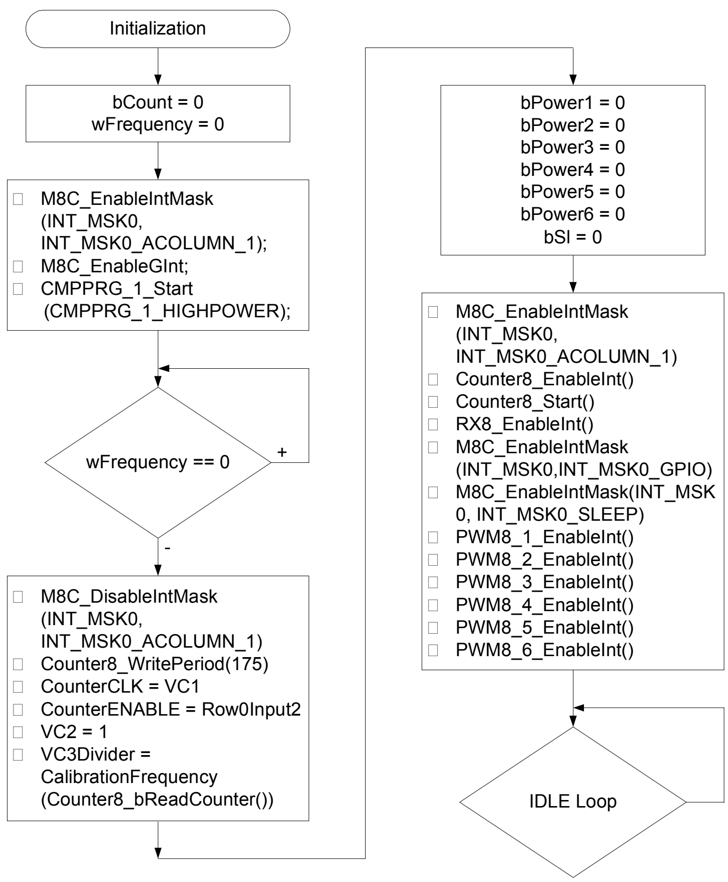


Figure 9. PSoC Initialization Flowchart

AC line frequency calibration is carried out only when the device is turned on and is intended to adjust TRIAC turn-on angle setting appropriately for the utilized line frequency.

There are 255 lamp brightness levels. The value of the PWM generator period is set constant and equal to 256 clock pulses. The VC3 divider supplies the clock. The duration of the PWM period must be equal to exactly ½ of AC line period (Figure 10).

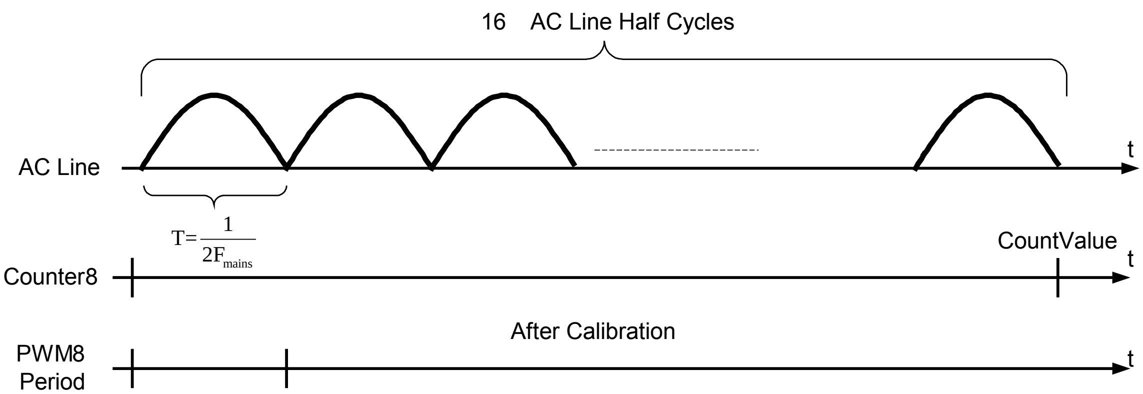


Figure 10. Calibration Procedure

This is done by tuning the VC3 divider during the calibration procedure. It operates in the following way: Counter8 starts counting during 16 AC line zero-crossing comparator interrupts (16 half cycles). The count value is used for VC3 divider calculation in the C*alibrationFrequency()* routine using the following formulas:

$$\frac{Cnt_{Value}}{Cnt_{Clock}} = \frac{1}{2 \cdot f} \quad (1)$$

$$\frac{256}{PWM_{Clock}} = \frac{1}{2 \cdot f} \quad (2)$$

$$\frac{Cnt_{Value}}{Cnt_{Clock}} = \frac{256}{PWM_{Clock}} \quad (3)$$

$$VC_3 = \frac{Cnt_{Value} \cdot VC_3^{cal}}{256} \quad (4)$$

$VC3^{cal}$, the value during the calibration procedure, is set to 100 and f is the AC line frequency.

For increased measurement precision, the calibration procedure integrates 16 half cycles of the AC line frequency. For correct Counter8 and PWM8 during these 16 half cycles, the clock frequency is reduced by a factor of 16 by setting VC2 = 16 instead of the normal value VC2=1.

wFrequency is a flag that shows that calibration has competed. Once the program starts, this flag is reset and the AnalogColumn1 interrupts are enabled. The flag reset is done in the master program by the AnalogColumn1 interrupt handler. After that, the values of the necessary dividers are set and Counter8 settings are modified for use as a break detector.

At the second part of PSoC initialization, the variables and necessary modules for device initialization are carried out. First, the variables, which contain the brightness of each lamp, are reset. Next, the necessary interrupt permission flags are set and two modules start: Counter8 and CMP. When the break signal passes over the DMX line, the Counter8 interrupt handler is brought in. The *wAddressCounter* variable is reset and the RX8 is restarted in the Counter8 interrupt handler (Figure 11).

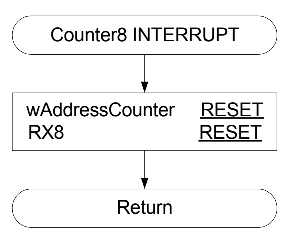


Figure 11. Counter8 Interrupt Flowchart

The GPIO is used for the zeroing of Counter8 (this is in the absence of an enable signal on the Counter8). See Figure 12.

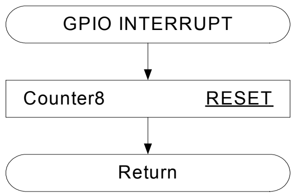


Figure 12. GPIO Interrupt Flowchart

The SleepTimer interrupt handler flowchart is shown in Figure 13.

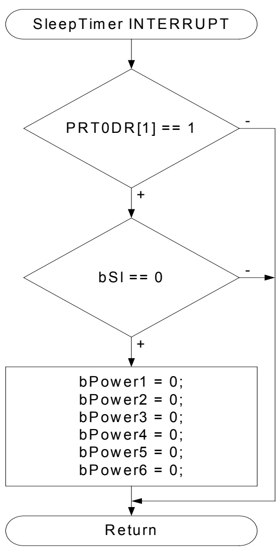


Figure 13. SleepTimer Interrupt Flowchart

Initialization of the variables that contain lamp brightness value is done under the following conditions: DMX bus sleep-mode support switched ON and interrupt handler is not set from RX8 *bSI* flag during the one-second time-out period.

The AnalogColumn1 interrupt handler from the comparator bus consists of two functions. First the device relative to the AC line frequency is calibrated and second, the PWMs are initiated. The flowchart of the AnalogColumn1 interrupt handler is shown in Figure 14. Once the *wFrequancy* flag is cleared (calibration has not yet occurred), incrementation of the bCount counter is done. When the counter value is equal to zero, the Counter8 starts. When the counter value is equal to 16, the Counter8 stops and the calibration completion flag is set.

If calibration was done, the interrupt handler from the comparator stops all PWMs and sets PulseWidth of all PWMs according to preset lamp brightness (which is saved in the *bPower1-6* variables in main.c).

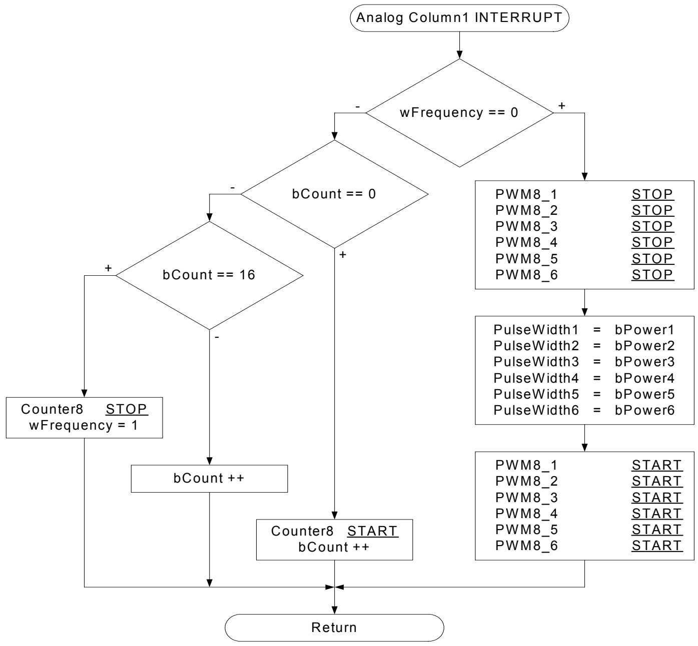


Figure 14. AnalogColumn1 Interrupt Flowchart

If the data byte enters from the DMX line, the RX8 interrupt handler is invoked (see Figure 15). It reads the data and status bytes. If wCountAddress contains more than 512 channels, or errors in the byte status are detected (OverrunError, FramingError), the RX8 stops. Counter8 is used to restart the RX8 interrupt handler. This means that a new data burst has entered. On the other hand (the value of address counter is correct and there are no errors), the device address is formed in the wSwitch variable and then compared with the value of the address counter. If the address of any lamp matches the value of the address counter, the data byte is put in the corresponding variable. After the comparison, the address counter is incremented.

The RX8 interrupt handler also sets the *bSI* flag, which means the DMX bus is active. If the value of lamp brightness is 255, the TRIACS will malfunction (because voltage of the AC line frequency is not enough to support the TRIAC ON state). Therefore, lamp brightness must be no greater than 254. The difference between 254 and 255 is 0.02%, which is imperceptible to the human eye.

In order to increase noise immunity (oscillations of electric supply network), all PWMs stop when their counter value is equal to zero. This triggers the TerminalCount interrupt handler for each PWM. This technique eliminates phase error accumulation caused by AC frequency measurement errors.

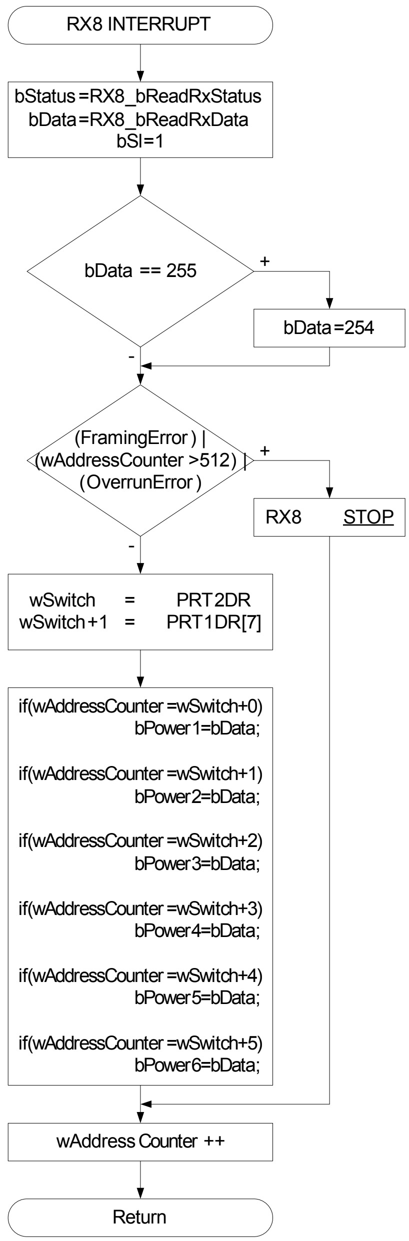


Figure 15. RX8 Interrupt Flowchart

TRIAC Control, Synchronization Signal Waveforms

Figure 16 shows the four waveforms collected.

- AC line frequency
- Signal on *AC Synchronizer* output (in Figure 5 it is called “F100”)
- Signal on PWM output
- TRIAC control pulse

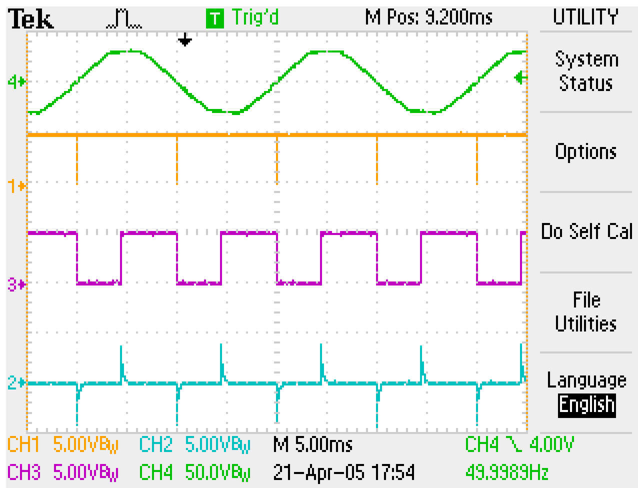


Figure 16. TRIAC Control and Synchronization Signal Waveforms

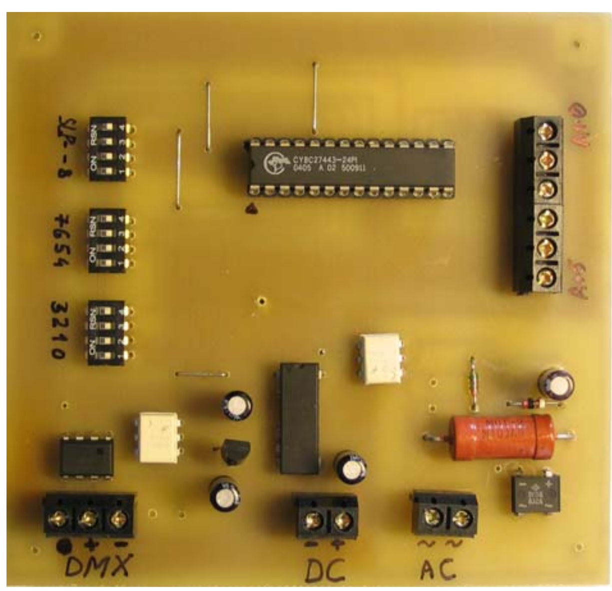


Figure 17. Board

Conclusion

The optimal structure for a multi-channel dimmer system (more than 6 channels) is a two-chip design (Figure 18). The DMX Protocol receiver can be implemented using the low-cost, CY8C21xxx PSoC device family. The 16-channel PWM generator can be built using the CY8C29xxx family or even a software implemented multi-channel PWM generator. In this case, the second chip can be from the CY8C21xxx family as well.

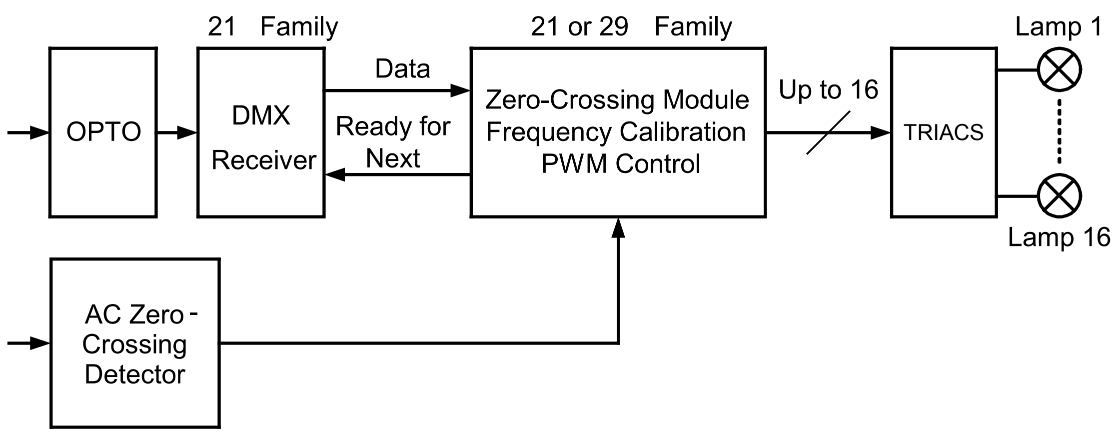


Figure 18. 16-Channel DMX System

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