



Application Note

AN2345

Simple Method to Generate Digital Signals with Variable Phase Shift Between

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Associated Part Family: All, Except 25/26
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Associated Application Notes: No

Abstract

This Application Note describes a simple method to generate digital signals with variable phase shift between the signals in the range of 0 – 360 degrees. The described method is very simple because it requires only one digital block per generated signal. The associated project for two signals is also described.

Introduction

Often it is necessary to obtain several digital signals with some phase shift between them that can be changed during operation. These signals are usually used in quadrature receivers, impedance meters, full-bridge switch regulators, and motor control systems. There are several methods to obtain these signals and solve this task. Each of them has advantages and disadvantages. Let's consider the most common of these methods.

The first of these methods consists of generating needed signals entirely with software. This method does not require hardware and allows flexible control of signal parameters. The disadvantage is this method consumes all the processor's time, which complicates interrupt handling.

The second of these methods is DDS (Direct Digital Synthesis). This method uses a phase accumulator and DAC. The advantages of this method are high frequency support and phase resolution.

In this Application Note, a simple method to generate digital signals with variable phase shift is described. This method allows generation of up to 16 signals (depending to free PSoC® blocks) with phase variation for each of them. The advantage of the described method is it is accomplished with internal hardware and no software intervention. The disadvantage of this method is that, the generator must be stopped for a short period of time when making a change to the phase.

Theory of Generator Operation

To better understand how the generator operates, let's consider the internal details of the counter (see Figure 1). For further details, see the Counter User Module Data Sheet in PSoC Designer™ or the *PSoC Technical Reference Manual (TRM)* on <http://www.cypress.com>.

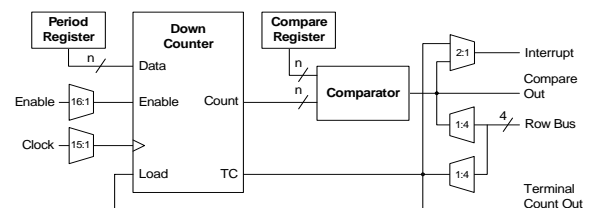


Figure 1. Counter Block Diagram

Once started, the counter operates continuously and reloads its internal value from the Period register upon reaching terminal count. During each clock cycle, the counter compares the current count to the value stored in the Compare register. When the counter is disabled and a period value is written into the Period register, the period value is also loaded into the down counter. When the counter is enabled, the counter counts down until terminal count (a count of 00h) is reached. On the next rising edge of the clock, the period is reloaded and, on subsequent clocks, counting continues.

The generator flowchart is shown in Figure 2.

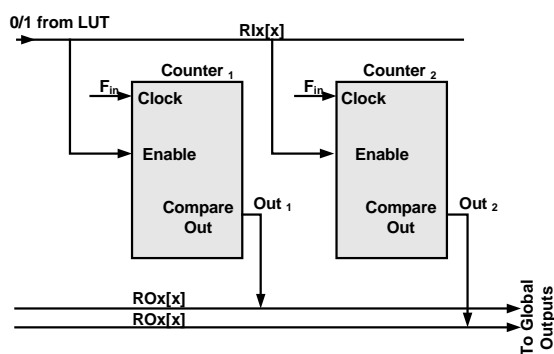


Figure 2. Generator Flowchart

The generator includes two counters: Counter₁ and Counter₂. During operation, the signals are generated on compare outputs of these counters. The same clock frequency F_{in} is connected to the clock inputs of the counters. The LUT signal is connected to the enable inputs via digital interconnect (not shown in Figure 2). This signal is controlled by software.

The main idea behind the generator lies in setting the first period shorter than the following periods by using a unique feature of counter operation. When the counters are stopped and disabled by a low enable signal, we load two different period values into their Period registers. These values are automatically copied to the down counter upon start of the counter. But because the enable signal is set low, the counters do not operate.

We now write the same period value to both counters. These values are copied to the corresponding down counter at the next underflow cycle. We can enable both counters simultaneously by setting the enable signal high. The counters then start operation, but because they were started from different initial counts, the underflow occurred at different times. Because the Period register contains the same value at this time, the equal output frequency will be generated with constant phase shift.

The timing diagrams, which illustrate this principle, are shown in Figure 3.

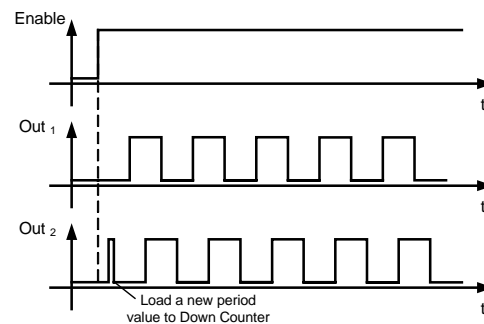


Figure 3. Generator Timing Diagram

Initialization of the generator is described as follows:

1. Set the enable signal to 0 and disable the counters.
2. Load the period and compare values into Counter₁.
3. Load the phase shift value into the Period register of Counter₂.
4. Call Counter_Start function for both counters. The values from the Period register are transferred to the down counter. The counter cannot start to count because there is no enable signal on the enable input.
5. Load the same period and compare values for Counter₁ into Counter₂.
6. Set the enable signal to 1 and enable the counters.

Source Code and PSoC Internals

The source code for initialization of the generator is shown below:

```
void Gen_start(BYTE Phase_shift)
{
//Stop counters
Counter8_1_Stop();
Counter8_1_Stop();

//LUT to false, Enable to low, counters are
stopped
RDI0LT1&=0x0F;

//Write to first counter period and comp.
value
Counter8_1_WritePeriod(199);
Counter8_1_WriteCompareValue(100);

//Write to second counter phase shift value
Counter8_2_WritePeriod(Phase_shift);

//Start counters
Counter8_1_Start();
Counter8_2_Start();

//Write to second counter period and comp.
value
Counter8_2_WritePeriod(199);
Counter8_2_WriteCompareValue(100);

//LUT true, Enable to high, counters are
started
RDI0LT1|=0xF0;
}
```

Code 1.

The period value P_{norm} can be calculated from Equation (1):

$$P_{norm} = \left[\frac{f_{clock}}{f_{des}} \right] - 1 \quad (1)$$

f_{clock} is the PWM clock frequency. f_{des} is the PWM output frequency.

The phase shift value P_{start} can be defined by Equation (2):

$$P_{start} = (P_{norm} + 1) \frac{\Delta\phi}{360^\circ} \quad (2)$$

P_{norm} is the PWM period for the expected output frequency. $\Delta\phi$ is the required phase shift, degrees.

The PSoC internal user module placement is shown in Figure 4.

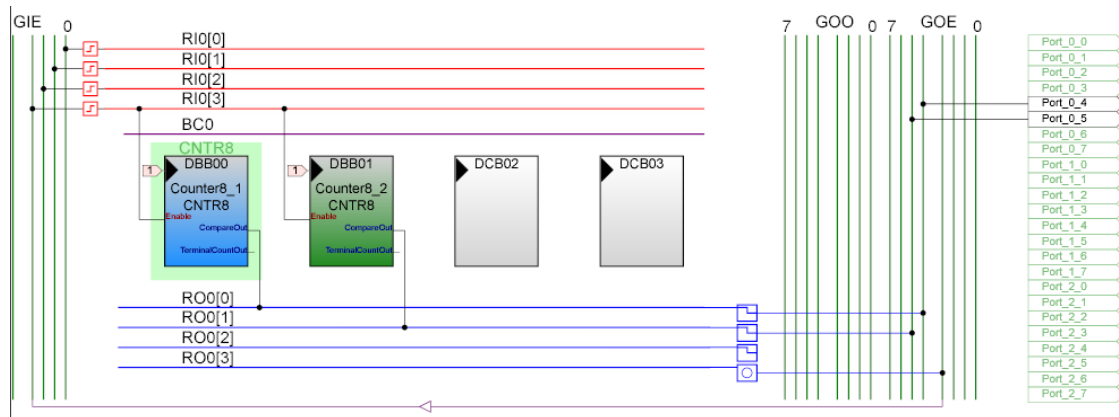
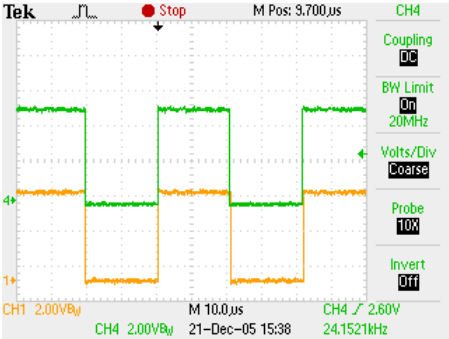


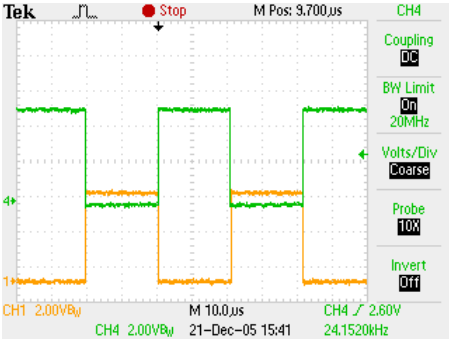
Figure 4. PSoC Internal User Module Configuration

The signal timing diagrams with different phase shifts are shown in the figure below. The upper waveform is the Counter₁ output signal. The lower waveform is the Counter₂ output signal.

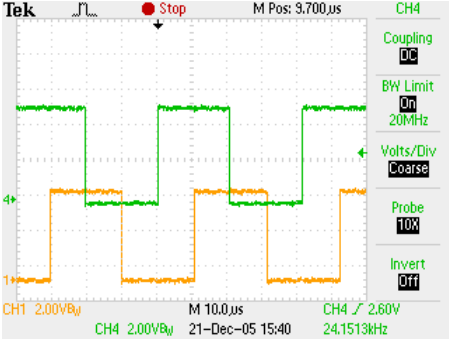
$$P_{norm} = 199.$$



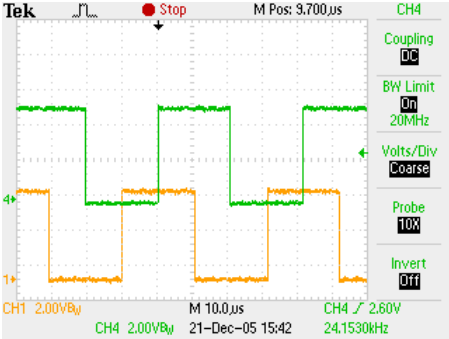
$P_{start} = 0$, Phase Shift=0°



$P_{start} = 100$, Phase Shift=180°



$P_{start} = 50$, Phase Shift=90°



$P_{start} = 150$, Phase Shift=270°

Figure 5. Scope Images

Conclusion

In this Application Note, the method to generate digital signals with variable phase shift between them is considered. This method allows generation of up to 16 signals with dynamic phase variation for each of them. Also, the project with two generated signals is demonstrated.

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